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1. **C++ encapsulated dynamic runtime power control for embedded systems**
Hernandez, O.J.; Dande, G.; Ofri, J.;
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8-10 April 2005 Page(s):126 - 130
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2. **EPIC: profiling the propagation and effect of data errors in software**
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5. **Skoll: distributed continuous quality assurance**
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1. **Techniques for minimizing and balancing I/O during functional partitioning**
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1. **Graph based communication analysis for hardware/software codesign**
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US 20050081130 A1	Using constrained scan cells to test integrated circuits	20050414	714/726	
US 20050076322 A1	System and method for lithography simulation	20050407	716/20	
US 20050076282 A1	System and method for testing a circuit design	20050407	714/739	
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US 20050065762 A1	ESD protection device modeling method and ESD simulation method	20050324	703/14	
US 20050057748 A1	Selecting a hypothetical profile to use in optical metrology	20050317	356/237.5	
US 20050042527 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20050224	430/5	
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US 20050015778 A1	Method and system for expressing the algorithms for the manipulation of hardware state using	20050120	719/321	
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US 20040252701 A1	Systems, processes and integrated circuits for rate and/or diversity adaptation for packet comi	20041216	370/395.21	
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209	713/330	
US 20040249915 A1	Advanced multi-network client device for wideband multimedia access to private and public wi	20041209	709/223	
US 20040243959 A1	Design method for semiconductor integrated circuit device	20041202	716/7	
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US 20040193390 A1	Method and apparatus for rapid evaluation of component mismatch in integrated circuit perfori	20040930	703/2	
US 20040193388 A1	Design time validation of systems	20040930	703/1	
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US 20020011949 A1	Golf course yardage and information system with zone detection	20020131	342/357.06
US 20020010544 A1	Display monitor for golf cart yardage and information system	20020124	701/213
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US 6845494 B2	Method for generating design constraints for modules in a hierarchical integrated circuit desig	20050118	716/6
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US 6832251 B1	Method and apparatus for distributed signal processing among internetworked wireless integr:	20041214	709/224
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US 6801220 B2	Method and apparatus for adjusting subpixel intensity values based upon luminance character	20041005	345/694
US 6792563 B1	Method and apparatus for bus activity tracking	20040914	714/43
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US 6785876 B2	Design method for semiconductor integrated circuit device	20040831	716/7
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6779157 B2	Semiconductor integrated circuit manufacturing method and model parameter extracting meth	20040817	716/2
US 6777141 B2	Phase shift mask including sub-resolution assist features for isolated spaces	20040817	430/5
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US 6758676 B2	Interactive education system for teaching patient care	20040706	434/262
US 6757645 B2	Visual inspection and verification system	20040629	703/13
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US 6751583 B1	Hardware and software co-simulation including simulating a target processor using binary trar	20040615	703/17
US 6742165 B2	System, method and computer program product for web-based integrated circuit design	20040525	716/1
US 6735743 B1	Method and apparatus for invalid state detection	20040511	716/4
US 6735630 B1	Method for collecting data using compact internetworked wireless integrated network sensors	20040511	709/224
US 6734509 B2	Semiconductor integrated circuit	20040511	257/393
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US 6704895 B1	Integrated circuit with emulation register in JTAG JAP	20040309	714/726
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US 6668337 B2	Method for designing integrated circuit based on the transaction analyzing model	20031223	714/6
US 6658633 B2	Automated system-on-chip integrated circuit design verification system	20031202	716/5
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US 6629296 B1	Functional verification of integrated circuit designs	20030930	716/5
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US 6615389 B1	Database for designing integrated circuit device, and method for designing integrated circuit d	20030902	716/1
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US 6615199 B1	Abstraction factory in a base services pattern environment	20030902	706/50
US 6610449 B2	Phase shift masking for "double-T" intersecting lines	20030826	430/5
US 6606744 B1	Providing collaborative installation management in a network-based supply chain environment	20030812	717/174

US 6606721 B1	Method and apparatus that tracks processor resources in a dynamic pseudo-random test prog	20030812	714/728
US 6606660 B1	Stream-based communication in a communication services patterns environment	20030812	709/227
US 6606609 B1	Apparatus and method for operating an integrated circuit	20030812	706/1
US 6606588 B1	Design apparatus and a method for generating an implementable description of a digital syste	20030812	703/15
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US 6601234 B1	Attribute dictionary in a business logic services environment	20030729	717/108
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US 6578187 B2	Digital circuit design method using programming language	20030610	716/18
US 6578068 B1	Load balancer in environment services patterns	20030610	709/203
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US 6551844 B1	Test assembly including a test die for testing a semiconductor product die	20030422	438/14
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US 6546505 B1	Processor condition sensing circuits, systems and methods	20030408	714/30
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US 6539522 B1	Method of developing re-usable software for efficient verification of system-on-chip integrated	20030325	716/5
US 6539497 B2	IC with selectively applied functional and test clocks	20030325	714/30
US 6539396 B1	Multi-object identifier system and method for information service pattern environment	20030325	707/103R
US 6529948 B1	Multi-object fetch component	20030304	709/217
US 6529909 B1	Method for translating an object attribute converter in an information services patterns environ	20030304	707/10
US 6526462 B1	Programmable multi-tasking memory management system	20030225	710/242
US 6525690 B2	Golf course yardage and information system with zone detection	20030225	342/357.13
US 6524752 B1	Phase shift masking for intersecting lines	20030225	430/5
US 6523157 B1	Method for designing integrated circuit device and database for design of integrated circuit dev	20030218	716/10
US 6522985 B1	Emulation devices, systems and methods utilizing state machines	20030218	702/117
US 6519754 B1	Methods and apparatuses for designing integrated circuits	20030211	716/18
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US 6505147 B1	Method for process simulation	20030107	703/2
US 6503666 B1	Phase shift masking for complex patterns	20030107	430/5
US 6503087 B1	Interactive education system for teaching patient care	20030107	434/262
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US 6496850 B1	Clean-up of orphaned server contexts	20021217	709/203
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US 6449761 B1	Method and apparatus for providing multiple electronic design solutions	20020910	716/11
US 6446239 B1	Method and apparatus for optimizing electronic design	20020903	716/2
US 6442748 B1	System, method and article of manufacture for a persistent state and persistent object separat	20020827	717/108
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US 6421251 B1	Array board interconnect system and method	20020716	361/788
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US 6389577 B1	Analyzing CMOS circuit delay	20020514	716/4
US 6389498 B1	Microprocessor having addressable communication port	20020514	710/268
US 6389379 B1	Converification system and method	20020514	703/14
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US 6370492 B1	Modified design representation for fast fault simulation of an integrated circuit	20020409	703/13
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US 6339836 B1	Automated design partitioning	20020115	716/5
US 6336087 B1	Method and apparatus for gate-level simulation of synthesized register transfer level design wi	20020101	703/15
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US 6311310 B1	Method and apparatus for wiring integrated circuits with multiple power buses based on perfor	20011030	716/2
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US 6285970 B1	Computer simulation method of silicon oxidation	20010904	703/2
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US 6263484 B1	Prototyping system and a method of operating the same	20010717	716/18
US 6240376 B1	Method and apparatus for gate-level simulation of synthesized register transfer level designs v	20010529	703/15
US 6240375 B1	Method of simulating an integrated circuit for error correction in a configuration model, and a c	20010529	703/14
US 6236940 B1	Display monitor for golf cart yardage and information system	20010522	701/300
US 6236360 B1	Golf course yardage and information system	20010522	342/357.13
US 6233540 B1	Design environment and a method for generating an implementable description of a digital sys	20010515	703/14
US 6233361 B1	Topography processor system	20010515	382/260
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic dev	20010410	716/1
US 6212493 B1	Profile directed simulation used to target time-critical crossproducts during random vector test	20010403	703/22
US 6212487 B1	Method and apparatus of establishing a region to be made amorphous	20010403	703/12
US 6208954 B1	Method for scheduling event sequences	20010327	703/16
US 6195790 B1	Electrical parameter evaluation system, electrical parameter evaluation method, and computer	20010227	716/20
US 6193152 B1	Modular signature and data-capture system and point of transaction payment and reward syste	20010227	235/380
US 6191663 B1	Echo reduction on bit-serial, multi-drop bus	20010220	333/17.3
US 6178533 B1	Method and system for design verification	20010123	714/739
US 6173240 B1	Multidimensional uncertainty analysis	20010109	703/2
US 6167491 A	High performance digital electronic system architecture and memory circuit therefor	20001226	711/149
US 6150724 A	Multi-chip semiconductor device and method for making the device by using multiple flip chip i	20001121	257/777
US 6134516 A	Simulation server system and method	20001017	703/27
US 6128718 A	Apparatus and method for a base address register on a computer peripheral device supporting	20001003	711/212
US 6117182 A	Optimum buffer placement for noise avoidance	20000912	716/8
US 6101276 A	Method and apparatus for performing two pass quality video compression through pipelining a	20000808	382/236

US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6078745 A	Method and apparatus for size optimization of storage units	20000620	717/151
US 6072994 A	Digitally programmable multifunction radio system architecture	20000606	455/84
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US 6061222 A	Method and apparatus for reducing noise in integrated circuit chips	20000509	361/111
US 6052706 A	Apparatus for performing fast multiplication	20000418	708/631
US 6038383 A	Method and apparatus for determining signal line interconnect widths to ensure electromigrati	20000314	716/5
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US 6023573 A	Apparatus and method for analyzing circuits using reduced-order modeling of large linear sub	20000208	703/2
US 6021266 A	Method of designing an integrated circuit using scheduling and allocation with parallelism and	20000201	716/2
US 6014570 A	Efficient radio signal diversity combining using a small set of discrete amplitude and phase we	20000111	455/500
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 6009255 A	Method of deposition profile simulation	19991228	703/6
US 6002861 A	Method for performing simulation using a hardware emulation system	19991214	703/16
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